CLAIMS

What is claimed is:

1. Circuitry for protection of an integrated circuit, which includes operational-circuits formed on a chip, the circuitry comprising:

a plurality of detectors, integrally formed on the chip as part of the integrated circuit and dispersed among the operational-circuits on the chip, the detectors being adapted, in response to radiation incident on the chip, to trigger a security measure so as to prevent tampering with the integrated circuit.

2. The circuitry according to claim 1, wherein the operational-circuits include components having predetermined circuit dimensions, and wherein the detectors are formed by modifying the circuit dimensions of one or more of the components so as to alter the response of the detectors to the radiation relative to the response of the operational-circuits that include the components having the predetermined circuit dimensions.

3. The circuitry according to claim 1, wherein the operational-circuits include components having predetermined doping, and wherein the detectors are formed by modifying the doping of one or more of the components so as to alter the response of the detectors to the radiation relative to the response of the operational-circuits that include the components having the predetermined doping.

4. The circuitry according to claim 1, wherein at least one of the detectors comprises a p-channel transistor coupled in series with an n-channel transistor, and wherein in response to the radiation a conductance of the p-channel transistor is substantially different from the conductance of the n-channel transistor.

5. The circuitry according to claim 1, wherein at least one of the detectors comprises a memory, and wherein the security measure comprises a change of state of the memory.

6. The circuitry according to claim 1, wherein the integrated circuit is implemented according to a technology chosen from at least one of metal oxide semiconductor and bipolar technologies.

7. The circuitry according to claim 1, wherein the chip is a semiconductor chip.

8. The circuitry according to claim 1, wherein the radiation comprises at least

one type of radiation chosen from electromagnetic radiation and ionizing radiation.

9. The circuitry according to claim 1, wherein the plurality of detectors are chosen from at least one biased-low detector which is operative to generate a logic low level in response to the radiation and at least one biased-high detector which is operative to generate a logic high level in response to the radiation.

10. The circuitry according to claim 1, and comprising a roughened chip surface that defocuses the radiation.

11. The circuitry according to claim 1, wherein the tampering comprises a fault being inserted into one of the operational-circuits so as to cause a functional result in the integrated circuit.

12. The circuitry according to any of claims 1-11, wherein the operational-circuits include components having predefined attributes, and wherein the detectors are formed by modifying at least one of the attributes of one or more of the components so as to alter the response of the detectors to the radiation relative to the response of the components having the predefined attributes.

13. The circuitry according to claim 12, wherein at least one of the detectors is coupled to serve as one of the components in one of the operational-circuits.

14. The circuitry according to claim 13, wherein the one of the operational-circuits functions according to predefined specifications while the radiation is not incident thereon.

15. The circuitry according to claim 14, wherein the one of the operational-circuits functions differently from the predefined specifications while the radiation is incident thereon.

16. The circuitry according to claim 12, wherein the components comprise transistors, and wherein the response of the detectors comprises an altered conductance of the transistors.

17. The circuitry according to claim 12, wherein the response of the detectors comprises a change in an operational level of the operational-circuits.

18. The circuitry according to claim 12, wherein the response of the detectors comprises a change in a signal timing of the operational-circuits.

19. The circuitry according to claim 12, wherein the predefined attributes are chosen from at least one of layout attributes, layout dimensions, manufacturing-process attributes, doping dosage, adding a sub-element of the component, removing the sub-element of the component, and materials type.

20. The circuitry according to any of claims 1-11, wherein the radiation comprises detector-triggering radiation, and wherein a level of the detector-triggering radiation is less than the level of radiation that affects a functionality of the operational-circuits while being sufficient to trigger the detectors.

21. The circuitry according to claim 20, wherein the radiation comprises optical radiation.

22. The circuitry according to any of claims 1-11, and comprising an auxiliary circuit which is coupled to at least one of the plurality of detectors and which is implemented to receive a trigger signal from the at least one of the detectors.

23. The circuitry according to claim 22, wherein the trigger signal is received as the security measure and wherein the auxiliary circuit is implemented to generate a control signal in response thereto, and comprising a control circuit which is coupled to receive the control signal so as to initiate an alarm in response thereto.

24. The circuitry according to claim 22, wherein the auxiliary circuit comprises elements selected from the operational-circuits and the detectors so as to provide an indication of the radiation in response to the radiation being incident on at least a part of the auxiliary circuit.

25. The circuitry according to claim 22, wherein the auxiliary circuit comprises a memory, and wherein the indication comprises a change of state of the memory.

26. The circuitry according to claim 22, wherein the auxiliary circuit has an asymmetric response to the radiation, and is implemented to convey an indication of the radiation to a signal receiver regardless of the radiation on the auxiliary circuit.

27. The circuitry according to any of claims 1-11, and comprising one or more auxiliary circuits coupled to at least one of the detectors and having an asymmetric response to the radiation.

28. The circuitry according to claim 27, wherein the one or more auxiliary circuits comprise a biased-low auxiliary circuit configured to output a logic low level in

response to the radiation and a biased-high auxiliary circuit configured to output a logic high level in response to the radiation, and wherein the biased-low auxiliary circuit and the biased-high auxiliary circuit are connected in series.

29. The circuitry according to any of claims 1-11, wherein the plurality of detectors comprises a memory comprising at least one of a biased-low detector which is operative to generate a logic low level in response to the radiation and a biased-high detector which is operative to generate a logic high level in response to the radiation.

30. Circuitry according to claim 29, and comprising the biased-low detector and the biased-high detector coupled in series.

31. A method for protection of an integrated circuit, which includes operational-circuits formed on a chip, the method comprising:

integrally forming a plurality of detectors on the chip as part of the integrated circuit, so that the detectors are dispersed among the operational-circuits on the chip, the detectors being adapted, in response to radiation incident on the chip, to trigger a security measure so as to prevent tampering with the integrated circuit.

32. The method according to claim 31, wherein the operational-circuits include components having predetermined circuit dimensions, and wherein the detectors are formed by modifying the circuit dimensions of one or more of the components so as to alter a response of the detectors to the radiation relative to a response of the operational-circuits that include the components having the predetermined circuit dimensions.

33. The method according to claim 31, wherein the operational-circuits include components having predetermined doping, and wherein the detectors are formed by modifying the doping of one or more of the components so as to alter a response of the detectors to the radiation relative to a response of the operational-circuits that include the components having the predetermined doping.

34. The method according to claim 31, wherein at least one of the detectors comprises a p-channel transistor coupled in series with an n-channel transistor, and wherein in response to the radiation a conductance of the p-channel transistor is substantially different from the conductance of the n-channel transistor.

35. The method according to claim 31, wherein at least one of the detectors comprises a memory, and wherein the security measure comprises a change of state of

the memory.

36. The method according to claim 31, wherein the integrated circuit is implemented according to a technology chosen from at least one of metal oxide semiconductor and bipolar technologies.

37. The method according to claim 31, wherein the chip is a semiconductor chip.

38. The method according to claim 31, wherein the radiation comprises at least one type of radiation chosen from electromagnetic radiation and ionizing radiation.

39. The method according to claim 31, and comprising choosing the plurality of detectors from at least one biased-low detector which is operative to generate a logic low level in response to the radiation and at least one biased-high detector which is operative to generate a logic high level in response to the radiation.

40. The method according to claim 31, and comprising roughening a chip surface so as to defocus the radiation.

41. The method according to claim 31, and comprising coupling an auxiliary circuit to at least one of the plurality of detectors and which is implemented to receive a trigger signal from the at least one of the detectors.

42. The method according to claim 31, wherein tampering comprises inserting a fault into one of the operational-circuits so as to cause a functional result in the integrated circuit.

43. The method according to any of claims 31-42, wherein the radiation comprises detector-triggering radiation, and wherein a level of the detector-triggering radiation is less than the level of radiation that affects a functionality of the operational-circuits while being sufficient to trigger the detectors.

44. The method according to claim 43, wherein the radiation comprises optical radiation.

45. The method according to any of claims 31-42, and comprising providing an auxiliary circuit which is coupled to at least one of the plurality of detectors and which is implemented to receive a trigger signal from the at least one of the detectors.

46. The method according to claim 45, wherein the trigger signal is received as the security measure and wherein the auxiliary circuit is implemented to generate a

control signal in response thereto, and comprising coupling a control circuit to receive the control signal so as to initiate an alarm in response thereto.

47. The method according to claim 45, wherein the auxiliary circuit comprises elements selected from the operational-circuits and the detectors so as to provide an indication of the radiation in response to the radiation being incident on at least a part of the auxiliary circuit.

48. The method according to claim 47, wherein the auxiliary circuit comprises a memory, and wherein the indication comprises a change of state of the memory.

49. The method according to claim 45, wherein the auxiliary circuit has an asymmetric response to the radiation, and is implemented to convey an indication of the radiation to a signal receiver regardless of the radiation on the auxiliary circuit.

50. The method according to any of claims 31-42, and comprising coupling one or more auxiliary circuits to at least one of the detectors, the auxiliary circuits having an asymmetric response to the radiation.

51. The method according to claim 50, wherein the one or more auxiliary circuits comprise a biased-low auxiliary circuit configured to output a logic low level in response to the radiation and a biased-high auxiliary circuit configured to output a logic high level in response to the radiation, and wherein the biased-low auxiliary circuit and the biased-high auxiliary circuit are connected in series.

52. The method according to any of claims 31-42, wherein the plurality of detectors comprises a memory comprising at least one of a biased-low detector which is operative to generate a logic low level in response to the radiation and a biased-high detector which is operative to generate a logic high level in response to the radiation.

53. The method according to claim 52, wherein the memory comprises the biased-low detector and the biased-high detector coupled in series.

54. A method for protection of an integrated circuit, which includes operational-circuits formed on a semiconductor chip, the operational-circuits including components having predefined attributes, the method comprising:

modifying at least one of the attributes of one or more of the components so as to alter a response of the one or more of the components to radiation; and

coupling the one or more of the components to the operational circuits to serve

as a detector, so as to trigger a security measure in response to radiation incident on the chip in order to prevent tampering with the integrated circuit.

55. The method according to claim 54, wherein the components comprise transistors, and wherein the response of the one or more of the components comprises an altered conductance of the transistors.

56. The method according to claim 54, wherein the response of the one or more of the components comprises a change in an operational level of the operational-circuits.

57. The method according to claim 54, wherein the response of the one or more of the components comprises a change in a signal timing of the operational-circuits.

58. The method according to claim 54, and comprising choosing the at least one of the predefined attributes from at least one of layout attributes, layout dimensions, manufacturing-process attributes, doping dosage, adding a sub-element of the component, removing the sub-element of the component, and materials type.

59. The method according to any of claims 54-58, wherein at least one of the operational-circuits functions according to predefined specifications while the radiation is not incident thereon.

60. The method according to claim 59, wherein the at least one of the operational-circuits functions differently from the predefined specifications while the radiation is incident thereon.

61.A method for protecting an integrated circuit, which includes operational-circuits formed on a chip, the method comprising:

providing circuitry, comprising a plurality of detectors, integrally formed on the chip as part of the integrated circuit and dispersed among the operational-circuits on the chip, the detectors being adapted, in response to radiation incident on the chip, to trigger a security measure so as to prevent tampering with the integrated circuit; and

activating the security measure.

62. The method according to claim 61, wherein the radiation comprises detector-triggering radiation which generates the security measure, and wherein a level of the detector-triggering radiation is less than the level of radiation that affects a functionality of the operational-circuits while being sufficient to trigger the detectors.

63. The method according to claim 61, and comprising modifying at least one of the operational-circuits to form at least one of the detectors, so that a response of the at least one of the detectors to the radiation is different from a response of the operational-circuits to the radiation.

64. The method according to claim 61, wherein the plurality of detectors are chosen from at least one biased-low detector which is operative to generate a logic low level in response to the radiation and at least one biased-high detector which is operative to generate a logic high level in response to the radiation.

65. An integrated circuit formed on a chip, comprising;

operational circuits comprising components having predefined attributes, wherein the attributes of a plurality of the components are modified so as to alter a response of the plurality of the components to radiation incident on the chip so as to prevent tampering with the integrated circuit.

66. A method for protection of an integrated circuit formed on a chip, the integrated circuit including operational-circuits including components having predefined attributes, the method comprising:

modifying the attributes of a plurality of the components so as to alter a response of the plurality of the components to radiation incident on the chip so as to prevent tampering with the integrated circuit.